

Octal 3-State Noninverting Buffer/Line Driver/ Line Receiver MC74HC244A, MC74HCT244A

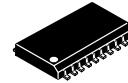
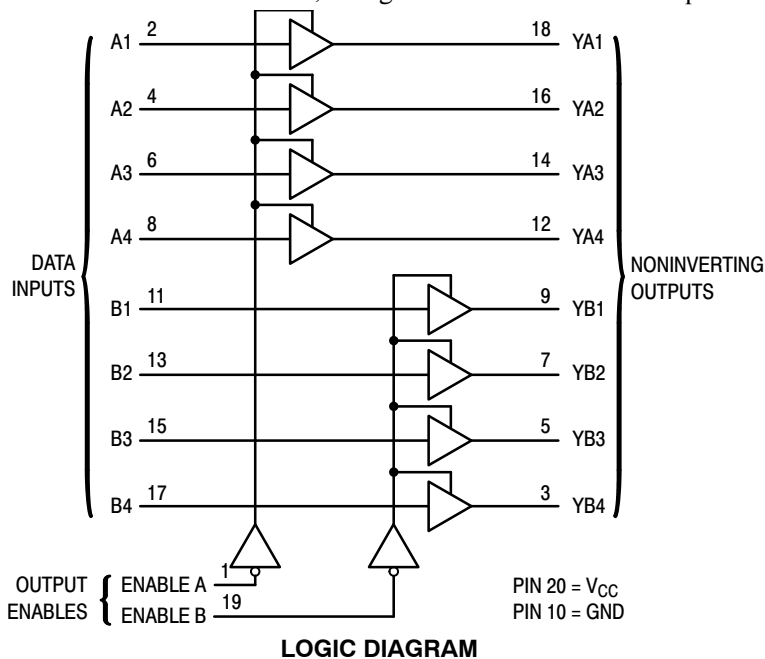
The MC74HC244A is identical in pinout to the LS244. The MC74HC244A device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The MC74HCT244A device inputs are compatible Standard CMOS or TTL outputs. The MC74HCT244A may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

These octal noninverting buffer/line drivers/line receivers are designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The devices have noninverting outputs and two active-low output enables.

The HC244A/HCT244A is the non-inverting version of the HC240A/HCT240A.

Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V (HC), 4.5 to 5.5 V (HCT)
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 136 FETs or 34 Equivalent Gates
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



SOIC-20
DW SUFFIX
CASE 751D

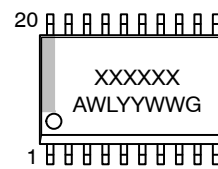


TSSOP-20
DT SUFFIX
CASE 948E

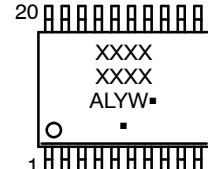
PIN ASSIGNMENT

ENABLE A	1	20	V _{CC}
A1	2	19	ENABLE B
YB4	3	18	YA1
A2	4	17	B4
YB3	5	16	YA2
A3	6	15	B3
YB2	7	14	YA3
A4	8	13	B2
YB1	9	12	YA4
GND	10	11	B1

MARKING DIAGRAMS



SOIC-20



TSSOP-20

- A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

Z = high impedance

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

MC74HC244A, MC74HCT244A

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +6.5	V
V_{IN}	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_{OUT}	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
I_{IK}	Input Clamp Current ($V_{IN} < 0$ or $V_{IN} > V_{CC}$)	± 20	mA
I_{OK}	Output Clamp Current ($V_{OUT} < 0$ or $V_{OUT} > V_{CC}$)	± 20	mA
T_{STG}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature Under Bias	± 150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC-20W 96 WQFN20 99 QFN20 111 TSSOP-20 150	°C/W
P_D	Power Dissipation in Still Air at 25°C	SOIC-20W 1302 WQFN20 1256 QFN20 1127 TSSOP-20 833	mW
MSL	Moisture Sensitivity	SOIC-20W Level 3 All Other Packages Level 1	-
F_R	Flammability Rating	Oxygen Index: 28 to 34 UL 94 V-0 @ 0.125 in	-
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model >2000 Charged Device Model N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
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MC74HC

V_{CC}	DC Supply Voltage	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Note 3)	0	V_{CC}	V
T_A	Operating Free-Air Temperature	-55	+125	°C
t_r, t_f	Input Rise or Fall Time	$V_{CC} = 2.0\text{ V}$ 0 $V_{CC} = 4.5\text{ V}$ 0 $V_{CC} = 6.0\text{ V}$ 0	1000 500 400	ns

MC74HCT

V_{CC}	DC Supply Voltage	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input Voltage, DC Output Voltage (Note 3)	0	V_{CC}	V
T_A	Operating Free-Air Temperature	-55	+125	°C
t_r, t_f	Input Rise or Fall Time	0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.



MC74HC244A, MC74HCT244A

DC ELECTRICAL CHARACTERISTICS (MC74HC244A)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				-55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} - 0.1 V I _{OUT} ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} - 0.1 V I _{OUT} ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL}					V
		I _{OUT} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	
		I _{OUT} ≤ 2.4 mA	3.0	2.48	2.34	2.2	
		I _{OUT} ≤ 6.0 mA	4.5	3.98	3.84	3.7	
V _{OL}	Minimum Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL}					V
		I _{OUT} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	
		I _{OUT} ≤ 2.4 mA	3.0	0.26	0.33	0.4	
		I _{OUT} ≤ 6.0 mA	4.5	0.26	0.33	0.4	
I _{IN}	Maximum Input Leakage Current	V _{IN} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{IN} = V _{IL} or V _{IH} V _{OUT} = V _{CC} or GND	6.0	±0.5	±5.0	±10	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = V _{CC} or GND	6.0	4.0	40	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (MC74HC244A)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			−55 to 25°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 2)	2.0	96	115	135	ns
		3.0	50	60	70	
		4.5	18	23	27	
		6.0	15	20	23	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to YA or B to YB (Figures 1 and 2)	2.0	110	140	165	ns
		3.0	60	70	80	
		4.5	22	28	33	
		6.0	19	24	28	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to YA or B to YB (Figures 1 and 2)	2.0	110	140	165	ns
		3.0	60	70	80	
		4.5	22	28	33	
		6.0	19	24	28	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0	60	75	90	ns
		3.0	23	27	32	
		4.5	12	15	18	
		6.0	10	13	15	
C _{IN}	Maximum Input Capacitance	–	10	10	10	pF
C _{OUT}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	–	15	15	15	pF
C _{PD}	Power Dissipation Capacitance (Per Enabled Output) (Note 4)	5.0	Typical @ 25°C			pF
			34			

4. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} \times V_{CC}^2 \times f + I_{CC} \times V_{CC}$.



MC74HC244A, MC74HCT244A

DC ELECTRICAL CHARACTERISTICS (MC74HCT244A)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} – 0.1 V I _{OUT} ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} – 0.1 V I _{OUT} ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL}					V
		I _{OUT} ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	
		I _{OUT} ≤ 6.0 mA	4.5	3.98	3.84	3.7	
V _{OL}	Minimum Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL}					V
		I _{OUT} ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	
		I _{OUT} ≤ 6.0 mA	4.5	0.26	0.33	0.4	
I _{IN}	Maximum Input Leakage Current	V _{IN} = V _{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{IN} = V _{IL} or V _{IH} V _{OUT} = V _{CC} or GND	5.5	±0.5	±5.0	±10	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = V _{CC} or GND	5.5	4.0	40	160	μA
ΔI _{CC}	Additional Quiescent Supply Current (Note 5)	V _{IN} = 2.4 V, Any One Input; V _{IN} = V _{CC} or GND, Other Inputs; I _{OUT} = 0 μA	5.5	≥ –55°C	25°C to 125°C		mA
				2.9	2.4		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

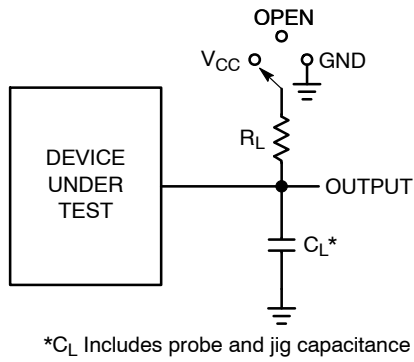
5. Total Supply Current = I_{CC} + Σ ΔI_{CC}.

AC ELECTRICAL CHARACTERISTICS (MC74HCT244A)

Symbol	Parameter	V _{CC} (V)	Guaranteed Limit			Unit
			–55 to 25°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 2)	4.5 – 5.5	20	25	30	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to YA or B to YB (Figures 1 and 2)	4.5 – 5.5	26	33	39	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to YA or B to YB (Figures 1 and 2)	4.5 – 5.5	22	28	33	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	4.5 – 5.5	12	15	18	ns
C _{IN}	Maximum Input Capacitance	–	10	10	10	pF
C _{OUT}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	–	15	15	15	pF

C _{PD}	Power Dissipation Capacitance (Per Enabled Output) (Note 4)	5.0	Typical @ 25°C	pF
			55	

MC74HC244A, MC74HCT244A



Test	Switch Position	C _L	R _L
t _{PLH} / t _{PHL}	Open	50 pF	1 kΩ
t _{PLZ} / t _{PZL}	V _{CC}		
t _{PHZ} / t _{PZH}	GND		

Figure 1. Test Circuit

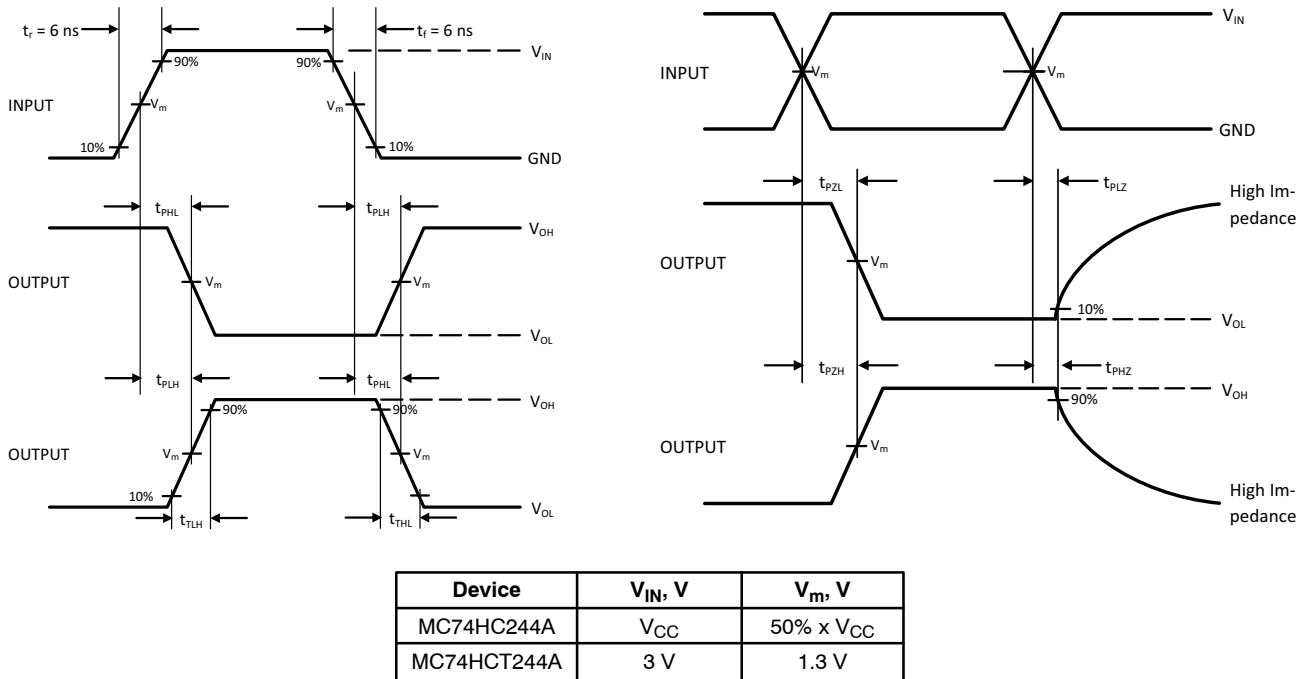


Figure 2. Switching Waveforms

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, B1, B2, B3, B4
(Pins 2, 4, 6, 8, 11, 13, 15, 17)

Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

Enable A, Enable B (Pins 1, 19)

Output enables (active-low). When a low level is applied to these pins, the outputs are enabled and the devices

function as noninverting buffers. When a high level is applied, the outputs assume the high impedance state.

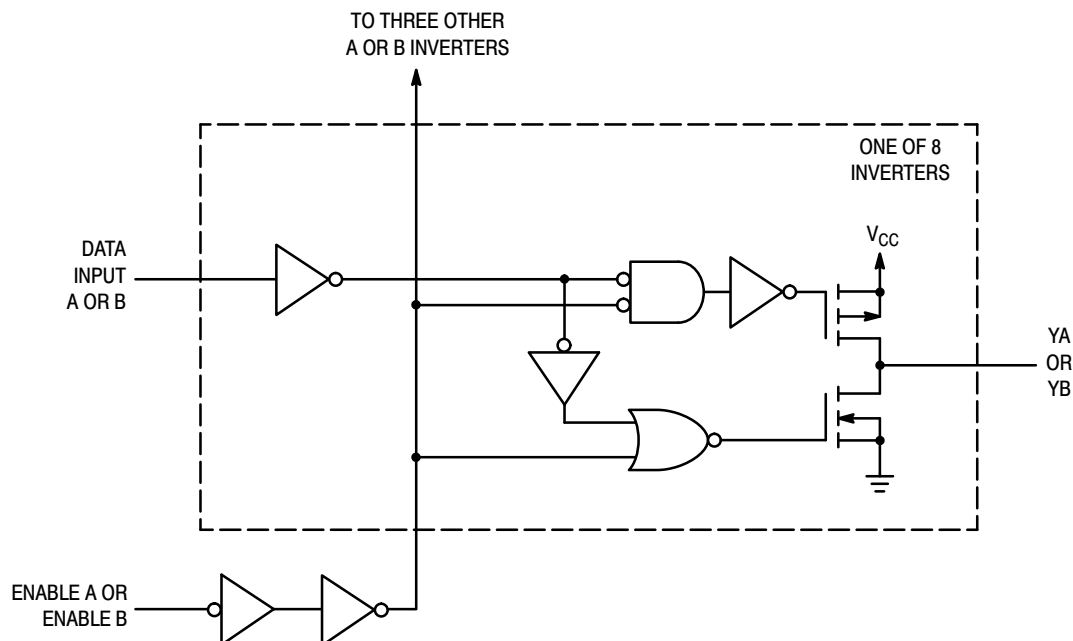
OUTPUTS

YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4
(Pins 18, 16, 14, 12, 9, 7, 5, 3)

Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high-impedance outputs.

MC74HC244A, MC74HCT244A

LOGIC DETAIL



ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
MC74HC244ADWG	HC244A	SOIC-20 WIDE	38 Units / Rail
MC74HC244ADWR2G	HC244A	SOIC-20 WIDE	1000 / Tape & Reel
MC74HC244ADWR2G-Q*	HC244A	SOIC-20 WIDE	1000 / Tape & Reel
MC74HC244ADTG	HC 244A	TSSOP-20	75 Units / Rail
MC74HC244ADTR2G	HC 244A	TSSOP-20	2500 / Tape & Reel
MC74HC244ADTR2G-Q*	HC 244A	TSSOP-20	2500 / Tape & Reel
MC74HCT244ADWG	HCT244A	SOIC-20 WIDE	38 Units / Rail
MC74HCT244ADWR2G	HCT244A	SOIC-20 WIDE	1000 / Tape & Reel
MC74HCT244ADWR2G-Q*	HCT244A	SOIC-20 WIDE	1000 / Tape & Reel
MC74HCT244ADTR2G	HCT 244A	TSSOP-20	2500 / Tape & Reel
MC74HCT244ADTR2G-Q*	HCT 244A	TSSOP-20	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

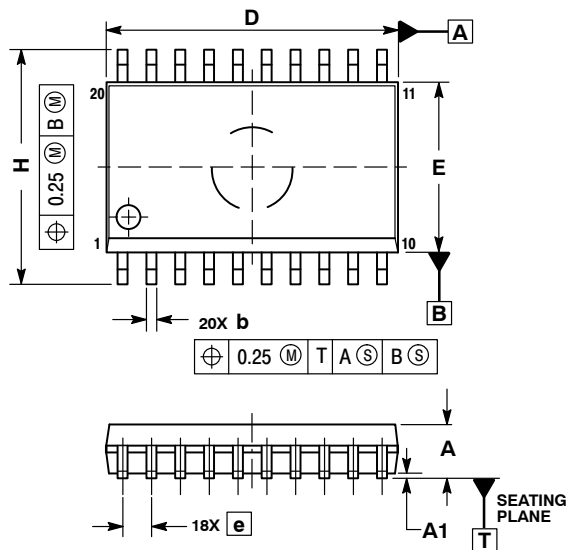
*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

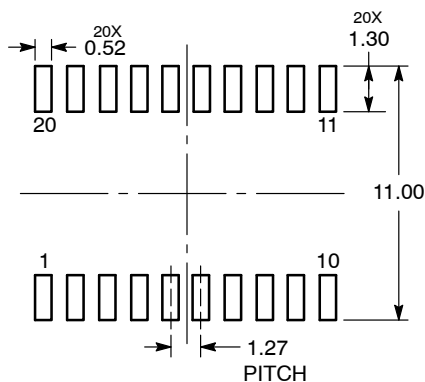
DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

RECOMMENDED
SOLDERING FOOTPRINT*



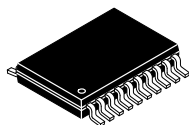
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

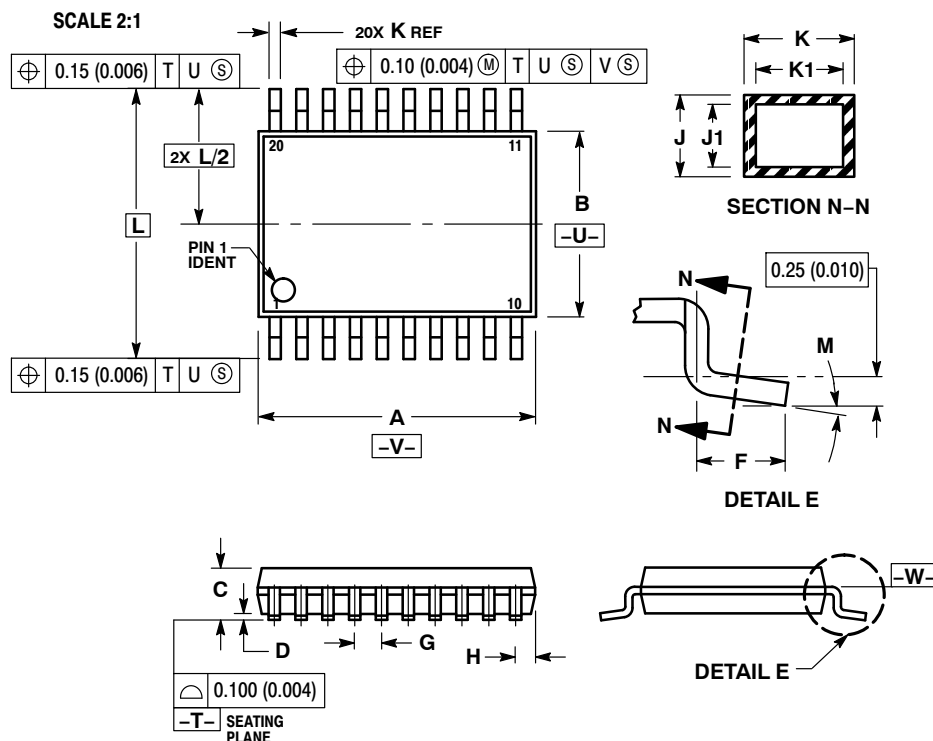
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TSSOP-20 WB
CASE 948E
ISSUE D

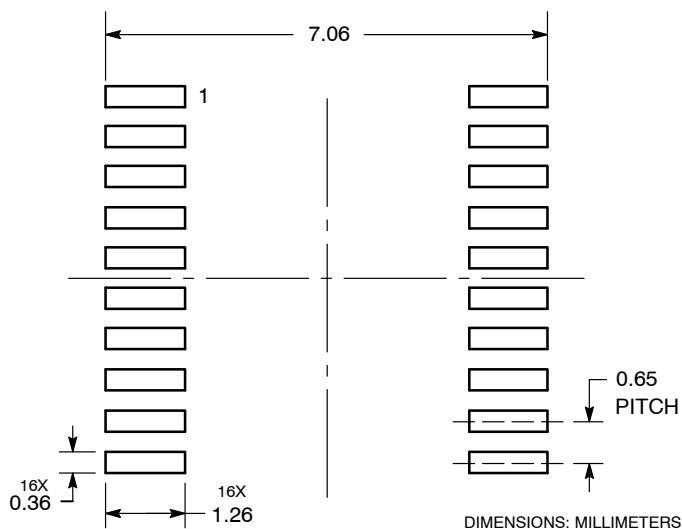
DATE 17 FEB 2016



- NOTES:**
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

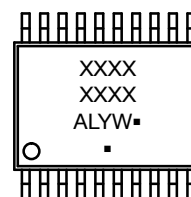
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**RECOMMENDED
SOLDERING FOOTPRINT***



*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual. SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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